

# Exhibit 24

PATENT  
Docket: 90065.052402 (17732.60750.00)  
Reply to Final Office Action of Oct. 27, 2003



## THE UNITED STATES PATENT & TRADEMARK OFFICE

REPLY UNDER 37 CFR 1.116 - EXPEDITED PROCEDURE - EXAMINING GROUP 2826

Applicant:	Grebs, et al.	)	
		)	
Serial No.:	10/247,464	)	
		)	Examiner: Abraham, Fetsum
Filed:	19 September 2002	)	
		)	Art Unit: 2826
For:	BURIED GATE FIELD	)	
	TERMINATION STRUCTURE	)	

## RESPONSE UNDER 37 CFR 1.116

Commissioner for Patents  
Mail Stop AF  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

In response to the Final Office Action mailed 27 October 2003, Applicants hereby submit the following Amendment in compliance with 37 CFR 1.121 as revised in the Final Rule: Changes to Implement Electronic Maintenance of Official Patent Application Records, 68 *Fed. Reg.* 38611 (June 30, 2003).


AF  
2800

Serial No.		Filing Date	Examiner	Group Art Unit
10/247,464		September 19, 2002	Abraham, Fetsum	2826

**CERTIFICATE OF MAILING BY FIRST CLASS MAIL (37 CFR 1.8)**  
Applicant(s): Thomas E. Grebs, et al.

Docket No.  
90065.052402/17732.60750.00

Invention: BURIED GATE - FIELD TERMINATION STRUCTURE




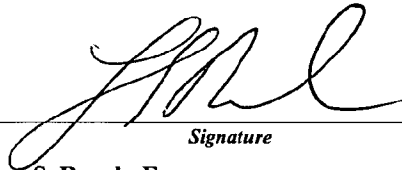
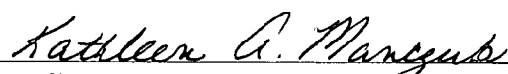
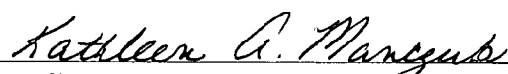
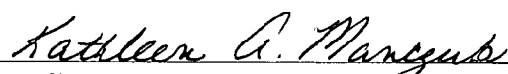
I hereby certify that this Response to Final Office Action (total 15 pages)  
(Identify type of correspondence)

is being deposited with the United States Postal Service as first class mail in an envelope addressed to:  
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on December 23, 2003  
(Date)

Kathleen A. Manczuk  
(Typed or Printed Name of Person Mailing Correspondence)

Kathleen A. Manczuk  
(Signature of Person Mailing Correspondence)

Note: Each paper must have its own certificate of mailing.

<b>AMENDMENT TRANSMITTAL LETTER (Large Entity)</b>				Docket No. <b>90065.052402/17732.60750.00</b>							
Applicant(s): <b>Thomas E. Grebs, et al.</b>											
Serial No. <b>10/247,464</b>	Filing Date <b>September 19, 2002</b>	Examiner <b>Abraham, Fetsum</b>		Group Art Unit <b>2826</b>							
Invention: <b>OBSTACLED GATE - FIELD TERMINATION STRUCTURE</b> 											
<u>TO THE COMMISSIONER FOR PATENTS:</u>											
Transmitted herewith is an amendment in the above-identified application.											
The fee has been calculated and is transmitted as shown below.											
<b>CLAIMS AS AMENDED</b>											
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST # PREV. PAID FOR	NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE						
TOTAL CLAIMS	12 -	24 =	0 x	\$18.00	\$0.00						
INDEP. CLAIMS	5 -	5 =	0 x	\$84.00	\$0.00						
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00						
<b>TOTAL ADDITIONAL FEE FOR THIS AMENDMENT</b>					<b>\$0.00</b>						
<input checked="" type="checkbox"/> No additional fee is required for amendment. <input type="checkbox"/> Please charge Deposit Account No. _____ in the amount of _____ <input type="checkbox"/> A check in the amount of _____ to cover the filing fee is enclosed. <input type="checkbox"/> The Director is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. <input type="checkbox"/> Any additional filing fees required under 37 C.F.R. 1.16. <input type="checkbox"/> Any patent application processing fees under 37 CFR 1.17.											
 Signature			Dated: <b>13-DEC-2003</b>								
<b>Laurence S. Roach, Esq.</b> <b>Registration No. 45,044</b> <b>Law Office of Thomas R. FitzGerald</b> <b>16 E. Main Street, Suite 210</b> <b>Rochester, NY 14614-1803</b> <b>Telephone: (585) 454-2250</b> <b>Fax: (585) 454-6364</b>			<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td colspan="2">I certify that this document and fee is being deposited on <b>Dec. 23, 2003</b> with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</td> </tr> <tr> <td colspan="2" style="text-align: center;">             Signature of Person Mailing Correspondence         </td> </tr> <tr> <td colspan="2" style="text-align: center;"> <b>Kathleen A. Manczuk</b>            Typed or Printed Name of Person Mailing Correspondence         </td> </tr> </table>			I certify that this document and fee is being deposited on <b>Dec. 23, 2003</b> with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.		 Signature of Person Mailing Correspondence		<b>Kathleen A. Manczuk</b> Typed or Printed Name of Person Mailing Correspondence	
I certify that this document and fee is being deposited on <b>Dec. 23, 2003</b> with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.											
 Signature of Person Mailing Correspondence											
<b>Kathleen A. Manczuk</b> Typed or Printed Name of Person Mailing Correspondence											
CC:											

P11LARGE/REV06

FAIR0017919

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## IN THE CLAIMS

1. (*Currently Amended*) A switchable semiconductor power device of the type which controls current conduction based on field effect principles, comprising:

a semiconductor layer having a transistor region including a source/drain formation and a termination region surrounding the transistor region, said termination region including an outer periphery corresponding to an edge of the device; and

a single conductor, configured for connection to a gate voltage supply, including first and second conductor portions with the first conductor portion **formed in a trench and being** positioned in the transistor region to control current flow through the source/drain formation and the second conductor portion positioned in the termination region, the second conductor portion:

including a contact for connection to the gate voltage supply; **and**

including a feed comprising conductive material formed in a trench extending along the outer periphery and around the transistor region, said feed electrically connecting the contact with the first conductor portion; and acting as a field plate to extend the device breakdown voltage in the termination region;

**and**

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20            **an isolation trench extending into the semiconductor layer and positioned between the edge of the device and the second conductor portion.**

2. (*Original*) The device of claim 1 further comprising a plurality of additional source/drain formations each configured with the first conductor portion in and about a trench region to provide a voltage-switchable conduction channel for controlling current flow through the semiconductor layer.

3 - 5. (*Canceled*)

6. (*Original*) The device of claim 1 wherein the transistor region comprises a vertical MOSFET device.

7 - 12. (*Canceled*)

13. (*Currently Amended*) ~~The method of claim 7 wherein the second trench is~~ **A semiconductor structure comprising:**  
**a layer of semiconductor material having an active device region and**  
**a peripheral region surrounding the active region;**

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- 5        a transistor device formed in the active region, and having a gate  
region including a gate conductor formed in a first trench, the gate  
conductor electrically isolated from the semiconductor layer by a relatively  
thin insulator; and
- 10        a second trench as deep or deeper than the first trench formed along  
the peripheral region and including a second conductor formed therein  
with a relatively thick insulator positioned to electrically isolate the second  
trench conductor from the semiconductor layer, said second conductor:  
electrically connected to the gate conductor of said transistor  
device; and
- 15        acting as a field plate to extend the device breakdown voltage  
in the termination region.

14 -15. (*Canceled*)

16. (*Currently Amended*) ~~The method of claim 14 wherein~~ A method  
for manufacturing a semiconductor device, comprising:  
providing on a layer of semiconductor material an active region and  
a termination periphery region surrounding the active region with a  
5        trenched transistor formation in the active region;

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forming a trenched gate runner in the termination region along the active region; and

forming first and second conductor regions such that said first and second conductor regions are electrically connected to form a continuous conductor with multiple regions and said first conductor region is in said trenched transistor formation and said second conductor region is said trenched gate runner such that said second conductor also acts as a field plate termination; wherein

the trenched gate runner extends further into the layer of semiconductor material than the trenched transistor formation.

17. (Currently Amended) ~~The method of claim 14 wherein~~ A method for manufacturing a semiconductor device, comprising:

providing on a layer of semiconductor material an active region and a termination periphery region surrounding the active region with a trenched transistor formation in the active region;

forming a trenched gate runner in the termination region along the active region, the trenched transistor formation ~~includes~~ including a gate conductor formed simultaneously with the gate runner by deposition of polysilicon; and



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10        **forming first and second conductor regions such that said first and**  
**second conductor regions are electrically connected to form a continuous**  
**conductor with multiple regions and said first conductor region is in said**  
**trenched transistor formation and said second conductor region is said**  
**trenched gate runner such that said second conductor also acts as a field**  
15 **plate termination.**

the trenched transistor formation **includes including** a gate conductor  
formed simultaneously with the gate runner by deposition of polysilicon

18. *(Canceled)*.

19. *(Original)* A semiconductor structure comprising:

a layer of semiconductor material having an active device region and a peripheral  
region surrounding the active region;

a transistor device formed in the active region including a plurality of  
5 source regions on one surface and drain region on the opposite surface;

a trench having an outer annular portion disposed in the peripheral region  
and enclosing the transistor device, the walls and the floor of the outer annular  
portion lined with an insulator and the outer annular portion filled with conductive  
material for forming a field plate around the transistor regions; and

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10 a plurality of elongated inner runners extending in the same direction  
across the one surface with the source regions and intersecting the outer annular  
portion at opposite ends of the runners, the runners having their floors and their  
walls lined with a gate insulating material and the runners filled with a conductor  
to form a gate structure in the transistor region to control current between the  
15 source regions and the drain.

20. (*Currently Amended*) The semiconductor of claim ~~[[22.]]~~ 19, wherein  
the conductor material comprises conductive polysilicon.

21. (*Currently Amended*) The semiconductor of claim ~~[[21]]~~ 20, further  
comprising a layer of metal on the conductive polysilicon.

22. (*Original*) The semiconductor of claim 20 wherein the insulator in the  
outer annular portion is thicker than the gate insulator in the runners.

23. (*Original*) The semiconductor of claim 20 wherein a common layer of  
conductive polysilicon fills the trench.

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24. (*Original*) The semiconductor of claim 24 further comprising a second layer of insulator over the polysilicon to cover the walls of the polysilicon in the annular trench and to cover the tops of the runner trenches.

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Reply to Final Office Action of Oct. 27, 2003**REMARKS**

Claims 1-4, 6-7 and 10-19 are pending in this application. Claims 13, 16 and 17 are objected to, and claims 1-4, 6-7, 10-12, 14-15 and 18-19 are rejected. Claims 3-4, 7, 10-12, 14-15, and 18 are canceled, and claims 1, 13, 16-17 and 20-21 are amended, hereby.

5        Claim 1 stands finally rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,998,833 (Baliga). Claim 1 is amended hereby, and Applicant respectfully traverses the rejection as applied thereto.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)(*Emphasis Added*). Applicant submits that the  
10        cited reference fails to disclose or suggest all the limitations of amended claim 1, and that therefore a *prima facie* case of obviousness has not been established in regard thereto.

Baliga discloses a gate trench (*not referenced*, Fig. 5) filled with a gate  
15        conductor material 126, and an edge termination trench (*not referenced*) lined with field plate insulating layer 134 and a field plate 136 is disposed upon layer 134.

In contrast, claim 1 as amended recites in part "a single conductor . . . including first and second conductor portions with the first conductor portion  
20        formed in a trench and being positioned in the transistor region . . . the second

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conductor portion . . . including a feed comprising conductive material formed in a trench extending along the outer periphery and around the transistor region” and “an isolation trench extending into the semiconductor layer and positioned between the edge of the device and the second conductor portion”. (Emphasis

5 *Added*). Thus, claim 1 has been amended to include the subject matter of original claims 3 and 4 (canceled hereby). More particularly, the structure recited in amended claim 1 includes gate trench 28 (*Fig. 1*), runner trench 58, each of which are filled with a single conductor, and an isolation trench 72 filled with insulation layer 36.

10 The Examiner indicates at Page 3, lines 5-7, that claims 3 and 4 were rendered obvious because the first conductor 126 of Baliga is formed in a trench and a portion of the isolation trench where the second conductor is positioned is between the conductor 136 and the edge of the structure. However, there is no indication of an isolation trench as formerly claimed in claim 4, and as now  
15 claimed in amended claim 1. Baliga discloses only two trenches, i.e., the gate and edge-termination trenches. Baliga does not include three trenches, nor does Baliga disclose or suggest an isolation trench with an isolation insulating layer disposed therein.

Thus, Baliga fails to disclose or suggest a single conductor including first  
20 and second conductor portions with the first conductor portion formed in a trench and being positioned in the transistor region, the second conductor portion

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including a feed comprising conductive material formed in a trench extending along the outer periphery and around the transistor region, and an isolation trench extending into the semiconductor layer and positioned between the edge of the device and the second conductor portion, as recited in part by amended

5 claim 1.

Since Baliga fails to disclose or suggest all the limitations of claim 1, Applicant submits that a *prima facie* case of obviousness has not been established and requests withdrawal of the rejection. Accordingly, Applicant submits that claim 1 and claims 2-4 and 6 depending therefrom, are now in  
10 condition for allowance, which is hereby respectfully requested.

Claims 2 and 11 were also rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,998,833 (Baliga). Applicant respectfully points out that claim 2 depends from claim 1, which is in condition for allowance for the reasons given hereinabove. Accordingly, claim 2 is also in condition for  
15 allowance which is hereby respectfully requested. In regard to claim 11, Applicant respectfully points out that claim 11 has been cancelled hereby. Accordingly, Applicant respectfully requests withdrawal of the rejection as applied thereto.

Claims 3 and 4 were also rejected under 35 U.S.C. §103(a) as being  
20 unpatentable over U.S. Patent No. 5,998,833 (Baliga). Applicant respectfully

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points out that claims 3 and 4 have been canceled hereby. Accordingly,  
Applicant respectfully requests withdrawal of the rejection as applied thereto.

Claims 6 and 10 were also rejected under 35 U.S.C. §103(a) as being  
unpatentable over U.S. Patent No. 5,998,833 (Baliga). Applicant respectfully

5 points out that claim 6 depends from claim 1, which is in condition for allowance  
for the reasons given hereinabove. Accordingly, claim 6 is also in condition for  
allowance which is hereby respectfully requested. In regard to claim 10,  
Applicants point out that claim 10 has been canceled hereby. Accordingly,  
Applicant respectfully requests withdrawal of the rejection as applied thereto.

10 Claim 7 was also rejected under 35 U.S.C. §103(a) as being unpatentable  
over U.S. Patent No. 5,998,833 (Baliga). Applicant respectfully points out that  
claim 7 has been canceled hereby and respectfully requests withdrawal of the  
rejection as applied thereto.

Claim 12 was also rejected under 35 U.S.C. §103(a) as being  
15 unpatentable over U.S. Patent No. 5,998,833 (Baliga). Applicant respectfully  
points out that claim 12 has been canceled hereby and respectfully requests  
withdrawal of the rejection as applied thereto.

Claim 14 was also rejected under 35 U.S.C. §103(a) as being  
unpatentable over U.S. Patent No. 5,998,833 (Baliga). Applicant respectfully  
20 points out that claim 14 has been canceled hereby and respectfully requests  
withdrawal of the rejection as applied thereto.

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Claim 15 was also rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,998,833 (Baliga). Applicant respectfully points out that claim 15 has been canceled hereby and respectfully requests withdrawal of the rejection as applied thereto.

5 Claim 18 was also rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,998,833 (Baliga). Applicant respectfully points out that claim 18 has been canceled hereby and respectfully requests withdrawal of the rejection as applied thereto.

10 Claim 19 was also rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,998,833 (Baliga). Applicant respectfully traverses and submits that a *prima facie* case of obviousness has not been established in regard thereto.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 15 981, 180 USPQ 580 (CCPA 1974)(*Emphasis Added*). Applicant submits that the cited reference fails to disclose or suggest all the limitations of claim 19, and that therefore a *prima facie* case of obviousness has not been established in regard thereto.

20 Claim 19 recites in part "a trench having an outer annular portion disposed in the peripheral region and enclosing the transistor device, . . . for forming a field plate around the transistor regions" and "a plurality of elongated inner runners



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extending in the same direction across the one surface with the source regions  
and intersecting the outer annular portion at opposite ends of the runners”.  
(*Emphasis Added*).

Baliga, as discussed above, fails to disclose or suggest inner runners that  
5 intersect at their opposite ends with the outer annular portion of a trench forming  
part of a field plate termination. Since Baliga fails to disclose or suggest all the  
limitations of claim 19, Applicant submits that a *prima facie* case of obviousness  
has not been established in regard thereto. Accordingly, Applicant submits that  
claim 19 and claims 20-24 depending therefrom are now in condition for  
10 allowance, which is hereby respectfully requested.

Further, Applicant respectfully points out that in the Final Office Action the  
status of claims 20-24 has not been indicated. In the Office Action of 16 May  
2003 (Paper No. 5), claims 20-24 were rejected under 35 U.S.C. §112, second  
paragraph. To Applicant's best knowledge, no other rejections were applied to  
15 claims 20-24 in that, or any subsequent, Office Action. In Applicant's response to  
that Office Action, Applicant submitted new figures (Figs. 4A-4B) and addressed  
the 35 U.S.C. §112, second paragraph, in two full paragraphs (i.e., paragraphs 3  
and 4 on page 9 of Applicant's response), presumably to the satisfaction of the  
Examiner. In light of the lack of an indicated status in regard to claims 20-24,  
20 Applicant respectfully requests that the finality of the present Office Action be  
withdrawn and a new non-final Office Action be issued.

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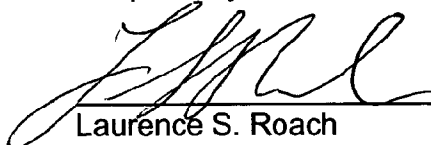
It should be noted that claims 20 and 21 have been amended herein to correct informalities therein. Applicant submits that claims 20 and 21 are now in allowable form.

For all the foregoing reasons, Applicant submits that the pending claims  
5 are definite and do particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Moreover, Applicant submits that no combination of the cited references teaches, discloses or suggests the subject matter of the pending claims. The pending claims are therefore in condition for allowance, and Applicant respectfully requests withdrawal of all rejections and  
10 allowance of the claims.

The Examiner is invited to telephone the undersigned in regard to this Amendment and the above identified application.

Respectfully submitted,

23-DEC-2003  
Date

  
Laurence S. Roach  
Reg. No. 45,044

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